

Docket No.: W&B-INF-1951

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : PETER BEER  
Filed : CONCURRENTLY HEREWITH  
Title : MEMORY CIRCUIT WITH A TEST MODE FOR WRITING TEST  
DATA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Sugibayashi, T. et al.: "A Distributive Serial Multi-Bit Parallel Test Scheme for Large Capacity DRAMs", IEICE Trans.Electron., Vol. E77-C, No. 4, August 1994, pp. 1323-1327.

Respectfully submitted,



For Applicant

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Date: October 1, 2003

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/nt/kf

<b>FORM PTO-1449 (SUBSTITUTE)</b>  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> (37 CFR 1.98(b))				Attorney Docket No.: W&B-INF-1951 Appl. No.:  <hr/> Applicant: PETER BEER  <hr/> Filing Date: October 1, 2003 Group Art Unit:			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
<b>FOREIGN PATENT DOCUMENT</b>							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
	J						
	K						
	L						
	M						
	N						
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
		Sugibayashi, T. et al.: "A Distributive Serial Multi-Bit Parallel Test Scheme for Large Capacity DRAMs", IEICE Trans.Electron., Vol. E77-C, No. 4, August 1994, pp. 1323-1327					
<b>EXAMINER</b>				<b>DATE CONSIDERED</b>			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							